Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently amended) The solid state imaging apparatus of claim 31, wherein one of two switching elements which are coupled to the first floating diffusion section ~~storage node~~ and one of two switching elements are coupled to the second floating diffusion section ~~storage node~~ are included in the same column.

3. (Currently amended) The solid state imaging apparatus of claim 31, wherein one of two switching elements which are coupled to the first floating diffusion section ~~storage node~~ and one of two switching elements which are coupled to the second floating diffusion section ~~storage node~~ are included in two adjacent columns.

4. (Currently amended) The solid state imaging apparatus of claim 35, wherein [[each]] said floating diffusion section ~~storage node~~ and [[each]] said pixel amplifier ~~output~~ transistor are shared by the two switching elements which are coupled to the first read line and the second read line, respectively.

5. (Currently amended) The solid state imaging apparatus of claim 35, further comprising:

a signal line for outputting a signal from said pixel amplifier ~~output~~ transistor to the outside; and

a select transistor which is provided between the pixel amplifier ~~output~~ transistor and the signal line.

6. (Currently amended) The solid state imaging apparatus of claim 35 [[34]], wherein the first floating diffusion section ~~storage node~~ and the pixel amplifier ~~output~~ transistor are shared by photoelectric elements which are adjacent to each other in the row direction or in the column direction.

7. (Currently amended) The solid state imaging apparatus of claim 31, further comprising:

a reset element for resetting charge stored in the first floating diffusion section ~~storage node~~.

8. (Previously presented) The solid state imaging apparatus of claim 31, wherein the photoelectric elements are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

9. (Currently amended) The solid state imaging apparatus of claim 35 [[33]], further comprising:

a signal processing circuit for processing an output signal from said pixel amplifier ~~output~~ transistor.

10. (Previously presented) The solid state imaging apparatus of claim 31, wherein:

the plurality of photoelectric elements arranged in an array of at least two rows and two columns define a unit of a photoelectric section; and

a plurality of the photoelectric sections are separated from one another by a power supply line which also functions as a light-shielding film.

11. (Canceled)

12. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photoelectric elements arranged in an array of at least two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to a first switching element which is coupled to a storage node, and a second read line coupled to a second switching elements which is coupled to the storage node,~~

wherein one of the pair of read lines is connected to a switching element at an odd-numbered column and the other is connected to a switching element at an even-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

13. (Currently amended) The solid state imaging apparatus of claim 12, further comprising:

a reset transistor for resetting charge stored in each said floating diffusion section ~~storage node~~ and ~~an output~~ a pixel amplifier transistor for detecting and outputting a voltage potential converted from said floating diffusion section ~~the storage node~~;

wherein a drain of the reset transistor is connected to a drain of the pixel amplifier ~~output~~ transistor so that the drain is shared by the reset transistor and the pixel amplifier ~~output~~ transistor.

14. (Currently amended) The solid state imaging apparatus of claim 12, wherein the floating diffusion section ~~storage node~~ is arranged between the two photoelectric elements which are adjacent to each other in the row direction.

15. (Currently amended) The solid state imaging apparatus of claim 13, wherein said switching elements are ~~transistor is~~ made of an MIS transistor, and

a gate of the MIS transistor is arranged in the row direction.

16. (Currently amended) The solid state imaging apparatus of claim 13, wherein said pixel amplifier ~~output~~ transistor is arranged between rows which include some of the photoelectric elements adjacent to each other.

17. (Currently amended) The solid state imaging apparatus of claim 13, wherein said pixel amplifier ~~output~~ transistor and said floating diffusion section ~~storage node~~ are arranged between the first read line and the second read line.

18. (Currently amended) The solid state imaging apparatus of claim 12, wherein the plurality of photoelectric elements arranged in an array of at least two columns ~~column~~ which define a photoelectric section; and [[the]] a pixel amplifier ~~output~~ transistor is arranged between the two photoelectric sections which are adjacent to each other in the column direction.

19. (Currently amended) The solid state imaging apparatus of claim 15, wherein each said pixel amplifier ~~output~~ transistor is arranged between the gate of a first MIS transistor and the gate of a second MIS transistor.

20. (Previously presented) The solid state imaging apparatus of claim 13, wherein each said reset transistor is arranged between the first read line and the second read line.

21. (Currently amended) The solid state imaging apparatus of claim 18, wherein the pixel amplifier ~~output~~ transistor and the floating diffusion section ~~storage node~~ are arranged between the two photoelectric sections which are adjacent to each other.

22. (Previously presented) The solid state imaging apparatus of claim 18, wherein said reset transistor is arranged between the two photoelectric sections, which are adjacent to each other in the row direction.

23. (Previously presented) The solid state imaging apparatus of claim 18, wherein said reset transistor is arranged between the two photoelectric sections, which are adjacent to each other in the column direction.

24. (Previously presented) The solid state imaging apparatus of claim 15, wherein said reset transistor is arranged between the gate of a first MIS transistor and the gate of a second MIS transistor.

25. (Currently amended) The solid state imaging apparatus of claim 18, wherein said floating diffusion section ~~storage node~~ is arranged between the two photoelectric sections which are adjacent to each other in the column direction.

26. (Previously presented) The solid state imaging apparatus of claim 12, wherein the photoelectric elements are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction.

27. (Currently amended) The solid state imaging apparatus of claim 13, wherein a line of the drain shared by the reset transistor and the pixel amplifier ~~output~~ transistor also functions as a light-shielding film.

28. (Currently amended) The solid state imaging apparatus of claim 13 [[12]], further comprising a signal processing circuit for processing an output signal from said pixel amplifier ~~output~~ transistor.

29. (Currently amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric elements arranged in an array of at leas two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~photosensitive devices to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to one of two switching elements which are coupled to a first storage node, and a second read line coupled to one of two switching elements which are coupled to a second storage node; and~~

~~said first read line also coupled to one of said two switching elements coupled to said second storage node, said second read line also coupled to one of said two switching elements coupled to said first storage node~~

wherein one of the pair of read lines connects between a switching element at an odd-numbered row and an odd-numbered column and a switching element at an even-numbered row

and an even-numbered column, and the other connects between a switching element at the odd-numbered row and the even-numbered column and a switching element at the even-numbered row and the odd-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

30. (Currently amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric elements arranged in an array of at least two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to a first switching element which are coupled to a storage node, and a second read line coupled to a second switching element which is coupled to the storage node~~

wherein one of the pair of read lines is connected to a switching element at an odd-numbered column and the other is connected to a switching element at an even-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

31. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photoelectric elements arranged in an array of at least two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to one of two switching elements which are coupled to a first storage node, and a second read line coupled to one of two switching elements which are coupled to a second storage node; and~~

~~said first read line also coupled to one of said two switching elements coupled to said second storage node, said second read line also coupled to one of said two switching elements coupled to said first storage node,~~

wherein one of the pair of read lines connects between a switching element at an odd-numbered row and an odd-numbered column and a switching element at an even-numbered row and an even-numbered column, and the other connects between a switching element at the odd-numbered row and the even-numbered column and a switching element at the even-numbered row and the odd-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction□

32-33. (Canceled)

34. (Previously presented) The solid state imaging apparatus of claim 3, wherein the plurality of photoelectric elements are photo diodes.

35. (Currently amended) The solid state imaging apparatus of claim 31, further comprising:

a pixel amplifier ~~an output~~ transistor which is coupled to the first floating diffusion section ~~storage node~~; and

the pixel amplifier ~~output~~ transistor comprises of a source follower transistor which detects and outputs a voltage potential converted from said [[the]] first floating diffusion section ~~storage node~~.

36. (Previously presented) The solid state imaging apparatus of claim 31, wherein the plurality of read lines are connected to a vertical scanning circuit.

37. (New) The solid state imaging apparatus of claim 12, further comprising:

a plurality of pixel amplifier transistors detecting and outputting a potential of the floating diffusion section, and

a plurality of a pair of signal lines outputting a signal from the pixel amplifier transistors to the outside,

wherein one of the pair of signal lines is connected to a pixel amplifier transistor which is adjacent to another pixel amplifier transistor in the row direction to which the other is connected.

38. (New) The solid state imaging apparatus of claim 31, further comprising:

a plurality of pixel amplifier transistors detecting and outputting a potential of the floating diffusion section, and

a plurality of a pair of signal lines outputting a signal from the pixel amplifier transistors to the outside,

wherein one of the pair of signal lines is connected to a pixel amplifier transistor which is adjacent to another pixel amplifier transistor in the row direction to which the other is connected.